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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,329	02/06/2002	John F. Gilsdorf	TRA-064	3149
36822 7590 01/26/2007 GORDON & JACOBSON, P.C. 60 LONG RIDGE ROAD SUITE 407 STAMFORD, CT 06902			EXAMINER MAIS, MARK A	
			ART UNIT 2616	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		01/26/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/072,329	Applicant(s) GILSDORF ET AL.	
	Examiner Mark A. Mais	Art Unit 2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 October 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 30, 2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4-7, 9-10, and 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Hann et al. (USP 6,535,520).

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4. With regard to claim 1, Hann et al. discloses a system for transferring synchronous [OC3 network, col. 1, line 56; fiber optic, col. 4, lines 56-57] and asynchronous signals [col. 1, line 57-58] between broadband access devices, said system comprising:

(a) at least two bus users [Fig. 1, PHYs 18 and the combination of interface 14 and PHYs 22];

(b) a data bus coupled to said at least two bus users [PHYs 18 and the combination of interface 14 and PHYs 22 are connected to a data bus, col. 4, lines 1-3];

(c) a clock bus coupled to said at least two bus users [it is inherent that PHYs 18 and 22 are coupled to a clock bus in order for them to be able to transfer data on a frame-based basis; *see also* col. 2, lines 54-67; e.g., frames 50 (Fig. 2), col. 4, line 67] ; and

(d) at least one control line coupled to said at least two bus users [Fig. 1, both Address 30 and CLAV 36 are coupled to both PHYs 18 and 22; they're interpreted as companion control lines completing a "handshake"], wherein

data is transferred between said at least two bus users over said data bus according to a repeating bus frame having a plurality of slots [e.g., frames 50 (Fig. 2), col. 4, line 67 and addresses 0-17], at least some of said plurality of slots being associated with asynchronous data streams [asynchronous slots which are arbitrated for by low speed units, addresses 1-7 and 9-17, col. 4, lines 16-17] and said at least one control line being asserted *whenever* valid data from one of said asynchronous data streams appears *on said data bus* in a slot of said repeating bus frame [Fig. 1, address 30 polls the asynchronous devices (addresses 1-7 and 9-17) for access to the data bus, col. 4, lines 4-9; CLAV line 36 goes to "1" when one of the low speed devices has data to transfer in it's assigned slot (address), col. 4, lines 32-40].

5. With regard to claim 4, Hann et al. discloses that the at least one control line includes a start of frame indicator which is asserted at the first slot of said repeating bus frame [Fig. 2, address #1 is the start of frame indicator; Fig. 1, address 30 polls the asynchronous devices (addresses 1-7 and 9-17) for access to the data bus, col. 4, lines 4-9; Fig. 2, CLAV 36 goes “high” or to “1” when one of the low speed devices has data to transfer in it’s assigned slot (address), col. 4, lines 32-40].

6. With regard to claim 5, Hann et al. discloses that at least one of said asynchronous data streams includes a repeating data frame [asynchronous slots which are arbitrated for by low speed units (and has data to transfer), addresses 1-7 and 9-17, col. 4, lines 16-17; frames 50 (Fig. 2), col. 4, line 67 and addresses 0-17], and the at least one control line includes a data frame indicator which is asserted when a slot in said repeating bus frame includes a start of frame indicator for said repeating data frame [Fig. 2, frame segment 1 is the data frame indicator; Fig. 2, address #1 is the start of frame indicator; Fig. 1, address 30 polls the asynchronous devices (addresses 1-7 and 9-17) for access to the data bus, col. 4, lines 4-9; Fig. 2, CLAV 36 goes “high” or to “1” when one of the low speed devices has data to transfer in it’s assigned slot (address), col. 4, lines 32-40]

7. With regard to claim 7, Hann et al. discloses that one of said at least two bus users is coupled to a SONET network [fiber optic is interpreted as SONET, col. 4, line 56] and another of said

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at least two bus users is coupled to a non-SONET network [ATM-based network, col. 1, lines 57-58].

8. With regard to claim 8, Hann et al. discloses that bus user coupled to the SONET network is the master [the master is interpreted as the combination of interface 14 and PHYs 22].

9. With regard to claim 9, Hann et al. discloses that bus user coupled to the non-SONET network is the master [the master is interpreted as the combination of interface 14 and PHYs 18] when the focus is on the transmit side (opposite of the receive side) [col. 7, lines 33-36].

10. With regard to claim 10, Hann et al. discloses a method for transferring synchronous [OC3 network, col. 1, line 56; fiber optic, col. 4, lines 56-57] and asynchronous signals [col. 1, line 57-58] between broadband access devices, said method comprising:

(a) generating a repeating bus frame having a plurality of slots [e.g., frames 50 (Fig. 2), col. 4, line 67 and addresses 0-17];

(b) associating at least some of said slots with asynchronous data streams [asynchronous slots which are arbitrated for by low speed units, addresses 1-7 and 9-17, col. 4, lines 16-17];

(c) transferring data between the broadband access devices *on a data bus* [PHYs 18 and the combination of interface 14 and PHYs 22 are connected to a data bus, col. 4, lines 1-3] according to the repeating bus frame [e.g., frames 50 (Fig. 2), col. 4, line 67 and addresses 0-17]; and

(d) asserting a first control line [Fig. 1, both Address 30 and CLAV 36 are coupled to both PHYs 18 and 22; they're interpreted as companion control lines completing a "handshake"], when valid data from one of the asynchronous data streams appears in a slot of the repeating bus frame [Fig. 1, address 30 polls the asynchronous devices (addresses 1-7 and 9-17) for access to the data bus, col. 4, lines 4-9; CLAV line 36 goes to "1" when one of the low speed devices has data to transfer in it's assigned slot (address), col. 4, lines 32-40].

11. With regard to claim 13, Hann et al. discloses

(e) asserting a second control line [Fig. 1, both Address 30 and CLAV 36 are coupled to both PHYs 18 and 22; they're interpreted as companion control lines completing a "handshake"] at the first slot of the repeating bus frame [Fig. 1, address 30 polls the asynchronous devices (addresses 1-7 and 9-17) for access to the data bus, col. 4, lines 4-9; CLAV line 36 goes to "1" when one of the low speed devices has data to transfer in it's assigned slot (address), col. 4, lines 32-40].

14. With regard to claim 14, Hann et al. discloses

(e) asserting a second control line [Fig. 1, both Address 30 and CLAV 36 are coupled to both PHYs 18 and 22; they're interpreted as companion control lines completing a "handshake"] when a slot of the repeating bus frame includes a framing signal of an asynchronous data stream [Fig. 1, address 30 polls the asynchronous devices (addresses 1-7 and 9-17) for access to the data bus, col. 4, lines 4-9; CLAV line 36 goes to "1" when one of the low speed devices has data to transfer in it's assigned slot (address), col. 4, lines 32-40].

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claims 2-3, 8, 11-12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hann et al.

17. With respect to claims 2-3 and 11-12, Hann et al. discloses a system for managing communications between low speed and high speed physical devices [**Abstract**]. Hann et al. also discloses that the physical devices are connected to a data bus [**col. 4, lines 1-3**]. Hann et al. discloses being able to handling disparate signals such as 2Mbps and 155 Mbps (and, accordingly, their companion slots/clock speeds) [**col. 2, lines 61-67**]. Hann et al. does not specifically disclose a specific slots/clock speed [i.e., 336/25 MHz or 1008/75 MHz]. However, Applicants have not disclosed that changing the slots/clock speed solves any stated problem or is for any particular purpose. It appears that the performance of the bus would result equally well with the system disclosed in Hann et al. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hann et al. to use the same

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slots/clock speed because such modifications are considered a mere design choice consideration, which fails to patentably distinguish over the prior art of Hann et al. In addition, changing the slots/clock speed is interpreted as an optimum value for a known process. A discovery of an optimum value for a known process is obvious engineering. See In re Aller, 105 USPQ 233 (CCPA 1955).

18. With respect to claims 6 and 15, Hann et al. discloses a system for managing communications between low speed and high speed physical devices [**Abstract**]. Hann et al. also discloses that the physical devices are connected to a data bus [**col. 4, lines 1-3**]. Hann et al. discloses being able to handling disparate signals such as 2Mbps and 155 Mbps (and, accordingly, their companion slots/clock speeds) [**col. 2, lines 61-67**]. Hann et al. does not disclose the length of each slot and the one bit position indicator the asynchronous slot. However, Applicants have not disclosed that changing length of each slot or the position indicator for the asynchronous slot solves any stated problem or is for any particular purpose. It appears that the performance of the bus would result equally well with the system disclosed in Hann et al. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hann et al. to use the same bit length of each slot or one bit position indicator bit for each asynchronous slot because such modifications are considered a mere design choice consideration, which fails to patentably distinguish over the prior art of Hann et al. In addition, changing the bit length of each slot or one bit position indicator bit for each asynchronous slot is interpreted as an optimum value for a known process. A discovery of an

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optimum value for a known process is obvious engineering. *See In re Aller*, 105 USPQ 233 (CCPA 1955).

Response to Arguments

19. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new grounds of rejection.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

(a) Pickett et al. (USP 5,339,395), Interface circuit for interfacing a peripheral device with a microprocessor operating in either a synchronous or an asynchronous mode.

(b) Borland et al. (USP 6,724,772), System-on-a-chip with variable bandwidth.

(c) Sheafor et al. (USP 6,119,188), Priority allocation in a bus interconnected discrete and/or integrated digital multi-module system.

(d) Upp (USP 6,104,724), Asynchronous data transfer and source traffic control system.

(e) Upp (USP 5,901,146), Asynchronous data transfer and source traffic control system.

(f) Wilson et al. (USP 5,150,359), Multiplexed synchronous/asynchronous data bus.

(g) Baxter et al. (USP 4,535,448), Dual bus communication system.

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(h) Kfir et al. (USP 6,996,125), Method and device for delivering communication in Ethernet-over-synchronous networks.

(i) Kulkarni et al. (USP 6,414,966), Bridging device for mapping/demapping Ethernet packet data directly onto and from a sonnet network.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Mais whose telephone number is 572-272-3138. The examiner can normally be reached on M-Th 5am-4pm.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MAM

January 4, 2006

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